IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of   Docket No: A8612

Pranav ASHAR , et al.

Appln. No.: Cont. of Serial No. 09/425,886

Confirmation No.: Not Yet Assigned   Group Art Unit: Not Yet Assigned

Filed: June 24, 2003   Examiner: Not Yet Assigned

For: FAST ERROR DIAGNOSIS FOR COMBINATIONAL VERIFICATION

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 CFR §1.56, Applicant hereby notifies

the U.S. Patent and Trademark Office of the documents which are listed on the attached

PTO/SB/08 A & B (modified) form which are all the references of record in parent application

No. 09/425,886. Applicant is not submitting duplicate copies of these references but requests

that they be listed on the face of any patent granted on the above application. (See

37 CFR §1.98(d)). Copies of any cited copending applications, if not previously submitted, are
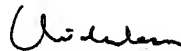
being submitted herewith.

The submission of the listed documents is not intended as an admission that any such

document constitutes prior art against the claims of the present application. Applicant does not

waive any right to take any action that would be appropriate to antedate or otherwise remove any

listed document as a competent reference against the claims of the present application.

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Respectfully submitted,

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Chidambaram Subramanian
Registration No. 43,355

WASHINGTON OFFICE

23373

PATENT TRADEMARK OFFICE

Date: June 24, 2003

Substitute for Form 1449 A & B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*		Application Number	Cont. of Serial No. 09/425,886
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		First Named Inventor	Pranav ASHAR et al.
		Art Unit	Not Yet Assigned
		Examiner Name	Not Yet Assigned
Sheet	1 of 2	Attorney Docket Number	A8612

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		Number	Kind Code[2] (if known)		
		US 5,831,996		11/03/1998	Abramovici et al.
		US 6,086,626		07/11/2000	Jain et al.
		US 6,138,266		10/24/2000	Ganesan et al.
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		US 5,506,852		04/09/1996	Chakradhar et al.

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Translation[6]
		Country Code[3]	Number[4]	Kind Code[5] (if known)			

OTHER ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	Translation[6]
		ABADIR, M., FERGUSON, J., KIRKLAND, Thomas E. "Logic Design Verification via Test Generation"; IEEE Translations on Computer Aided Design, vol. 7, no. 1, pp. 138-148, January 1988	
		BRYANT, R., "Graph-Based Algorithms for Boolean Function Manipulation, IEEE Translations On Computer, C-35(8); 677-691, August 1996	
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		KUEHLMANN, A.,; CHENG, D.,; SRINIVASAN, A.,; LAPOTIN, D.: "Error Diagnosis for Transistor-Level Verification", Proceedings of DAC, pp. 218-223, 1994.	
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		WATANABE, Y., BRAYTON, R., "Incremental Synthesis for Engineering Changes", Proceedings of ICCD, pp. 40-43, 1991	
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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		SENTOVICH, E., et al. "Sequential Circuit Design Using Synthesis and Optimization", Proceedings of ICCD, 1992	
		GUPTA, A., ASHAR, P., "Integrating a Boolean Satisfiability and BDDS for Combinational Verification, Proceedings of VLSI Design 98, pp. 222-225, 1998	
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		TOMITA, M., SUGANUMA, N., and HIRANO, K., "Pattern generation for locating logic design errors", IEICE Transactions Fundamentals, vol. E77-A, 1994	

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